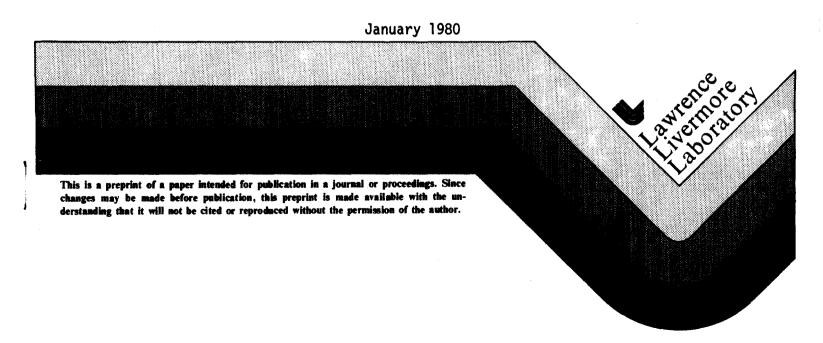
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2-D DIGITAL SIGNAL PROCESSING WITH AN ARRAY PROCESSOR

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2-D DIGITAL SIGNAL PROCESSING WITH AN ARRAY PROCESSOR

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ABSTRACT

The applicability of array processor (AP) technology to 2-D digital signal processing is investigated in this paper. The AP-based image processing facility at LLL is described, with emphasis on our applications software package which utilizes the array processor. Implementations of several key image processing algorithms are discussed and compared with other conventional processors, indicating that array processors are extremely cost-effective for image processing applications.

INTRODUCTION

One of the most important developments in the areas of high-speed scientific computing and distributed processing has been the recent introduction of the array processor. An AP is an arithmetic processor which, when connected to a host computer, provides extremely fast floating point computation. This is achieved via the use of parallel, pipelined floating point units and very fast registers, data memory, and program memory.

Digital image processing is an example of one application area particularly well-suited to array processor technology. This is due not only to the tremendous amount of numerical computation required, but also because most of the practical image processing algorithms are well-suited to implementation on a vector or parallel processor. In this paper we describe our efforts in developing a general purpose image processing facility which utilizes these capabilities of the array processor.

ARRAY PROCESSOR BASED IMAGE PROCESSING FACILITY

The Lawrence Livermore Laboratory is a national laboratory funded by the Department of Energy. The major emphasis at LLL is on the

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development of alternative energy sources and weapons research, although a large number of other programs also exist. In such an apolied physics setting, a number of applications have arisen requiring the processing of twodimensional imagery, or image processing [1]. Some of the image processing applications we have recently investigated include enhancement and restoration procedures for flash x-ray radiographs, enhancement of pinhole camera diagnostic images from laser fusion experiments and nuclear weapons tests, aerial surveillance for test ban treaty verification, decoding of Fresnel zone-plate coded images for laser diagnostics, ultrasonic imaging for hiological applications, and many others.

To provide effective image processing capabilities for such a diverse set of applications, we have developed an interactive minicomputer/array processor-hased image processing facility. A block diagram of our system is shown in Figure 1. Virtually all of the numerical computations required by the image processing algorithms are performed on the array processor, which is a Floating Point Systems AP120B with 16k of 167ns data memory (soon to be upgraded to 64k). The minicomputer, a PDP 11/70, serves primarily as a controller to drive the image display system, initiate array processor activity, and communicate with LLL's large computer network ("Octopus") consisting of several large mainframe computers.

One unique characteristic of our system as shown in Figure 1 is the existence of a direct data path between the array processor and the 80 megabyte system disks. This was achieved hy modifying both the array processor executive software (supplied by Floating Point Systems) and the PDP 11/70's operating system's disk driver software to allow for this "device to device" transfer. Such a configuration provides a very significant savings in input/output (I/O) requirements when compared with the more standard configuration of Figure 2a. This savings results for two reasons: 1) the larger amount of AP data memory (versus 11/70 available huffer) reduces the number of disk accesses required, and 2) the dual transfer of data (disk to host, then host to AP) required by the configuration of Figure 2a has been simplified to just one data transfer (disk to AP). Of course, an alternate method of achieving this savings is to purchase dedicated disks for the

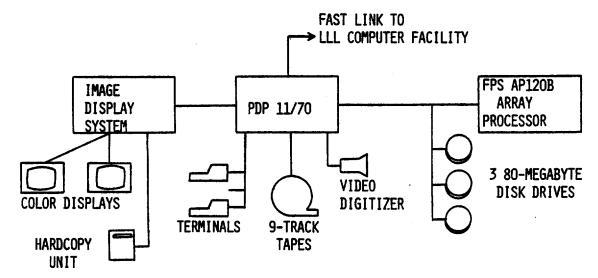
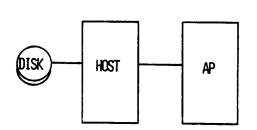
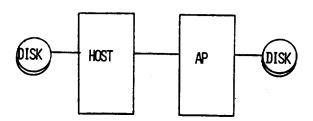


Figure 1. LLL's Image Processing Research Facility



a) Standard System Configuration



 b) System with Dedicated Disk(s) for AP Figure 2. Typical Array Processor System Configurations

AP, as shown in Figure 2b. By implementing our "device to device" transfer capability, however, we have avoided the increased capital investment (in the form of additional disks and an I/O processor for the AP) such a system would require.

2-D SIGNAL PROCESSING APPLICATIONS SOFTWARE

As indicated above, we are involved in a wide variety of applications at LLL requiring 2-D digital signal processing capabilities. Due to the diversity of the application needs, we have developed a general-purpose software system called "IMG" which implements a large number of fundamental image processing algorithms on our minicomputer and array processor. While there are too many routines to mention individually, most of the capabilities of IMG can be categorized as follows:

- Pointwise operators on images (includes add, substract, multiply, divide images; clip, exponentiate, log, absolute value, scale, and compute statistics on an image; histogram)
- 2) "Moving window" operators (includes median window filter, Wallis' contrast stretch algorithm [2], Lee's contrast stretch algorithm [3], nonrecursive filtering via convolution, derivatives, and average filter)
- Global operators (includes 2-D FFT, 2-D convolution via the FFT, alpha root, histogram equalization)
- Control functions (includes file name manipulation, file documentation via trailers, format conversions, image subsampling, image synthesis, and many others).

In addition, we are continuing to develop additional image processing software routines, many of which are based on the above fundamental operators. Examples include some linear and nonlinear filtering techniques and several image restoration algorithms, including Wiener restoration, spectral equalization, Frieden's iterative technique, and maximum entropy restoration. All of these software routines operate on disk-based images which, with a few exceptions such as radix-2 2-D FFT applications, are of arbitrary dimensions.

SOME IMPLEMENTATION AND AP PERFORMANCE ISSUES

A detailed discussion of the implementation issues encountered (e.g. CPU vs I/O effects, data memory size, algorithm vectorizability, etc.) in 2-D signal processing with an AP is well beyond the scope of the present paper. However, we will attempt to demonstrate the performance capabilities of the AP image processing package by briefly discussing a few key algorithms below.

<u>2-D FFT of Disk-based Images</u>: The 2-D FFT is, of course, one of the most important algorithms used in image processing. It is utilized in performing nonrecursive linear filtering, in several nonlinear filtering techniques, and in image restoration, to mention a few. The historical approach for computing 2-D FFT's of arrays larger than primary storage consists of decomposing the 2-D FFT into iterated 1-D FFT's. The calculation proceeds as follows: first each row in the array is transformed with the 1-D FFT. The array is then transposed and the row transform process is repreated (this computes the column transforms of the original array). This three-step procedure yields the transpose of the transformed array.

A significant part of the data manipulation required by the above procedure is a result of the matrix transpositions. A fast matrix transposition scheme, originally proposed by Eklundh in [4] and further extended in [5], provides an efficient (particularly in terms of 1/0) algorithm for transposing matrices of dimension $2^n \times 2^n$. An analysis of CPU and 1/0 requirements for 2-D digital filtering via the 2-D FFT with an array processor is given in [6], where the extended Eklundh method of matrix transposition was applied to the array processor system configuration of Figure 2a.

Two alternative schemes for computing the 2-D FFT without a matrix transposition have been developed in [7] and [8]. Careful examination of those algorithms, however, shows that they require exactly the same I/O procedure as Eklundh's matrix transposition scheme! This is a result of the similarity between data requirements for the matrix transposition and the column FFT. In fact, the 2-D FFT without matrix transposing may require slightly more I/O if the bit-reversed ordering of the rows that naturally results in the spatial frequency domain cannot be tolerated.

Until recently, the I/O scheme used in [4]-[5] and [7]-[8] for the implementation of 2-D FFTs (with or without matrix transposing) was the best available technique. A recently proposed "two-level" algorithm for matrix transposition, however, offers a significantly improved I/O scheme. This two-level technique is essentially Eklundh's method with a re-ordering of the sequence of computation, with the re-ordering resulting in fewer single-line transputs and hence fewer disk accesses. A detailed description of our array processor

·	2-0 FFT (512 x 512 real)	Contrast Stretch (512 x 512 Image, 2 x 2 Window)
PDP 11/70	122 sec (83, 39)	~3 minutes
PDP 11/70, AP120B with 16K mem.	18 sec (4.5, 13.5)	11.0 sec (7.0, 4.0)
PDP 11/70, AP120B with 64K mem.	~8 sec	~9.3 sec (7.0, 2.3)
CDC 7600 with 512K	3.3 sec (2.1, 1.2)	5.1 sec (3.9, 1.2)

TABLE 1. Comparative timings for 2 representative image processing algorithms on various comoputer systems. Approximate timings (~) denoted where hardware or software was insufficient for accurate timing. Below each time is given the (CPU, I/O) portion of the total.

implementation of this scheme for the 2-D FFT is given in [91. As noted in Table 1, our 512 x 512 FFT (with 16k AP data memory) requires only 18 seconds, providing highly interactive image processing. Upgrading to 64k of AP data memory will significantly decrease the FFT time, to about 8 seconds. The array processor implementation therefore far excels the minicomputer-alone implementation, and even approaches that of the CDC 7600. This is remarkable when one considers that the 7600, at about \$8 million, costs approximately 100 times as much as the array processor:

Contrast stretch algorithm: As noted above, we have implemented several "moving window" operators on our array processor. These image processing algorithms use the pixels in a ?-D neighborhood of the current input pixel to calculate the current output pixel. Examples of such algorithms are FIR filters and the median window filter. Typical window sizes range from 2 x 2 to 25 x 25 or larger, with the smaller windows heing of more interest for most practical image processing problems.

Wallis' contrast stretching algorithm [?] is one particularly effective moving-window enhancement technique. The algorithm is a nonlinear, image-dependent processor which equalizes the local mean and local variance throughout an image. Our array processor implementation of this algorithm, as shown in Table 1, requires only 11 seconds for a 2 x 2 window and a 512 x 512 image. Once again, the

array processor provides an interactive capability that approaches the performance of the far more expensive mainframe computer.

CONCLUSION

The LLL investigation into the application of array processors for interactive image processing has been summarized. Our image processing facility has been described, with emphasis on the role of the array processor. A brief discussion of algorithm implementations was given, with examples illustrating that the array processor can provide the computational throughput required for highly interactive image processing. For the typical image processing algorithms discussed, the array processor was found to deliver approximately 50% of the capability of a CDC 7600 at about 1% of the cost.

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